

A New Multilevel Inverter with Reduced Maximum Blocking Voltage

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ABSTRACT: This project proposes a new topology for cascaded multilevel inverters using reduced maximum blocking voltage technique. This can produce many levels with minimum number of power electronic switches. The proposed structure has some advantages including reduction in the number of switches, gate driver circuits, power diodes, and cost and installation area. The algorithm helps to determine the magnitude of dc sources. Equations are introduced for determining optimal voltage ratio of DC voltage for cascaded multilevel inverter which will maximum the number of voltage levels obtainable resulting in high power quality.

KEYWORDS: Multilevel inverter, Cascaded H Bridge, Maximum blocking voltage, Pulse Width Modulation.

I. INTRODUCTION

Nowadays, multilevel inverters are an attractive solution in the medium and high voltage applications. Such as high power quality, lower harmonic components, better electromagnetic consistence, lower dv/dt and lower switching losses. There are three main topologies and several derivation topologies for multilevel inverters. The main topologies are a) diode-clamped multilevel inverters, in this structure; the voltage balancing of Dc-link capacitors for higher levels is difficult. Moreover, the number of is high b) flying capacitor inverter: this topology needs a large number of capacitors for high voltage levels and balancing of the capacitor voltage is difficult. c) The H-bridge cascaded inverter this structure is the most important topology in comparison with two other classical topologies. The main advantage of these inverters is the low number of different voltage amplitude of used DC sources. In order, to increase the number of output levels with lower number of power semiconductor devices, different asymmetric cascaded multilevel inverter has been presented [5]. Several modulation techniques have been presented for multilevel inverter such as SPWM, SVPWM, and selective harmonic elimination. For proposed structures, the fundamental switching frequency is utilised.

II. PROPOSED TOPOLOGY

A new 11-level inverter structure has been proposed, this topology is generalised level multilevel inverter to produce output voltage waveform. In this structure, the bidirectional switches is easy to control, but its ON-state voltage drop is high. The structure of proposed symmetric multilevel inverter based on non-isolated voltage sources. This topology consists of basic unit and full bridge converter. The basic unit includes n bidirectional switches and n+1 dc voltage sources. The values of output voltage for different switching states in the recommended symmetric structure are illustrated in Table 1. Therefore, the number of IGBT (N_{IGBT}) is obtained using the following equation,

$$N_{IGBT} = 2n+2 \quad (1)$$

Where n represents the number of bidirectional switches of the proposed symmetric topology. Each bidirectional switches needs one gate driver circuits. Hence the number of number of gate drivers (N_{driver}) in the proposed topology is given by

$$N_{driver} = N_{level} + 1/2 \quad (2)$$

In this topology, the number of output voltage levels is obtained as follows

$$N_{level} = 2n+1 \quad (3)$$

$$N_{IGBT} = 2n+2 \quad (4)$$

The maximum output voltage ($V_{o, max}$) is given by

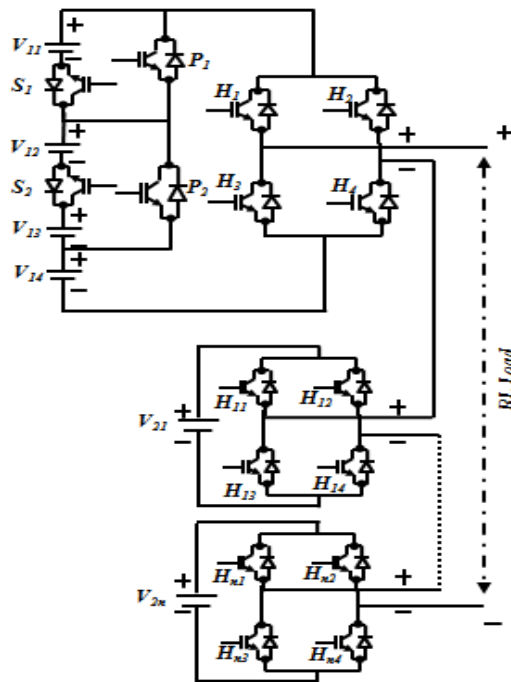
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$$V_{0max} = 2V_{dc} \quad (5)$$

This structure needs several DC voltage sources. The circuit consists of an AC voltage source, IGBT and the connected load is RL. It generates multiple DC voltage sources.



1.1 The generalised structure of symmetric proposed topology

Table1: Various Switching Pattern

State	Switching State												Output Voltage
	S ₁	S ₂	P ₁	P ₂	H ₁	H ₂	H ₃	H ₄	H ₁ '	H ₂ '	H ₃ '	H ₄ '	
0V	0	0	0	0	1	0	0	1	0	0	1	1	0
±1V	0	0	1	1	1	0	0	1	0	0	0	0	+V _{dc}
	0	0	1	1	0	1	1	0	0	0	0	1	-V _{dc}
±2V	1	0	0	1	1	0	0	0	0	0	0	0	+2V _{dc}
	1	0	0	1	0	1	0	0	0	0	0	1	-2V _{dc}
±3V	0	1	1	0	1	0	1	1	0	0	0	0	+3V _{dc}
	0	1	1	0	0	1	1	0	0	0	0	1	-3V _{dc}
±4V	1	1	0	0	1	0	0	1	0	0	0	0	+4V _{dc}
	1	1	0	0	0	1	1	0	0	0	0	1	-4V _{dc}
±5V	1	1	0	0	1	0	0	1	1	0	0	0	+5V _{dc}
	1	1	0	1	0	1	1	0	0	1	1	1	-5V _{dc}

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Block diagram for proposed topology

The pulse width modulation which carries the signal to generate the pulses into the gate driver circuits to the proposed multilevel inverter. The load and dc voltage sources are connected to the proposed system. The PWM technique is mainly used for the output voltage control can be obtained without any additional components and also with this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are minimized as higher order harmonics can be filtered easily.

III.COMPARISON WITH OTHER TOPOLOGIES

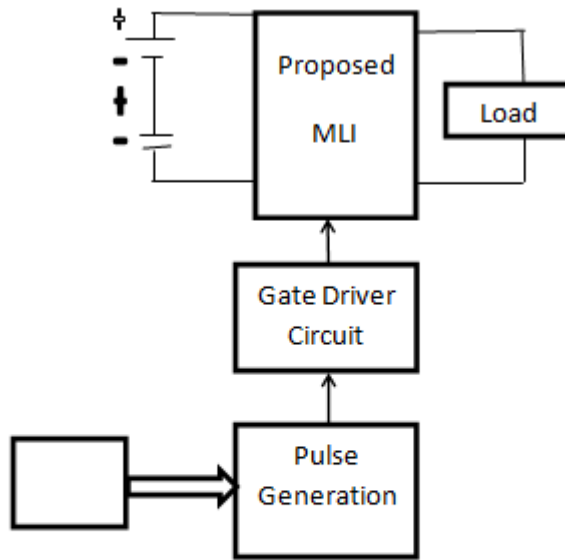


Fig. 2 Block diagram for proposed topology

In the symmetric H-bridge topology, for n dc voltage sources, the number of levels and the number of IGBTs are $2N_s + 1$ and $N_s + 5$, respectively. For the proposed topology, the number of levels and IGBTs are $2n + 1$ and $2n + 2$, respectively. Moreover, the number of levels and IGBTs of the proposed topology are $2n + 1$ and $2n + 2$, respectively. Fig. 1a shows the comparison between the proposed symmetric topology, symmetric H-bridge topology and the proposed symmetric structures in [6].

However, the number of IGBTs in the proposed topology is less than the symmetric H-bridge topology and proposed symmetric topology in [7]. The number of gate driver circuits and IGBTs in symmetric H-bridge topology and proposed symmetric topologies in [8] are equal. Fig. 2b compares the number of levels against blocking voltage. This figure shows that the commended structure needs minimum number of gate driver circuits. Gate driver circuits are the electronic part of the multilevel converter structure and the reduction of the number of gate drivers leads to simple control, lower cost and smaller size.

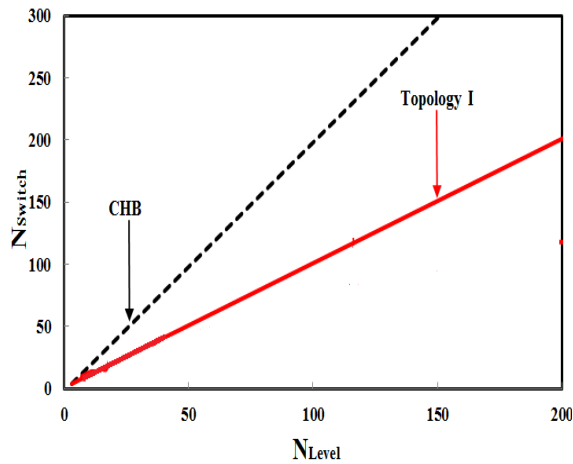


Fig.1a Comparison of Number of Level against number of switches

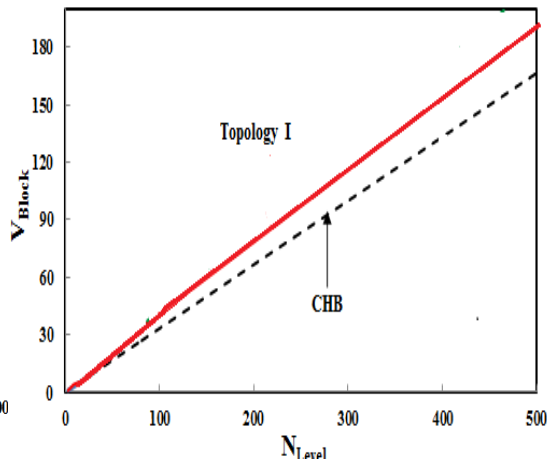


Fig.2b Comparison of level against Voltage blocking

Another important criterion in a multilevel inverter is the maximum voltage stress of the switches. It is shown in Fig 3a. For m dc voltage sources in the proposed symmetric topology, the maximum voltage stress of the full-bridge converter switches will be (mV_{dc}) and the maximum voltage stress of the bidirectional switch will be $(2V_{dc})$. The maximum voltage stress of all switches of the proposed symmetric topologies in [9] is (mV_{dc}) . Therefore the maximum voltage stress of the switches of the proposed topology is less than the maximum voltage stress of the switches of the proposed topology in the proposed symmetric topologies and it is an important advantage.

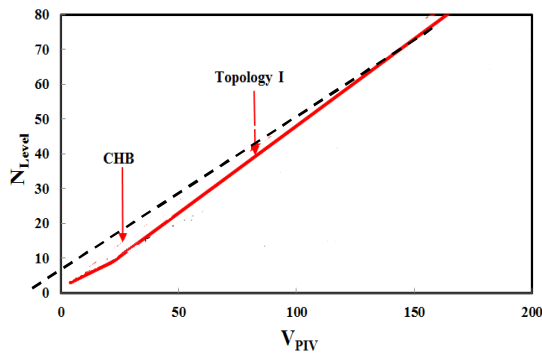


Fig.3a Comparison of Peak inverse voltage against Number of level

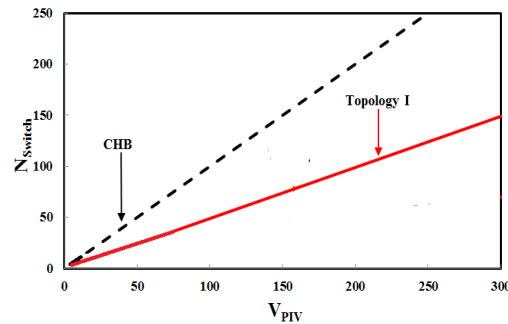


Fig.3b Comparison of Peak inverse voltage against Number of switches

Another comparison is occurs between number of switches against peak inverse voltage. Here the proposed symmetric topology has less number of switches therefore the peak inverse voltage also reduced when compared to symmetric H- bridge topology and it is shown in fig 3b. Now another comparison is made between the number of level against peak inverse voltage. Here, the proposed topology has less number switches when compared to cascaded H-bridge. So the peak inverse voltage also reduced when it compares to the cascaded H-bridge.

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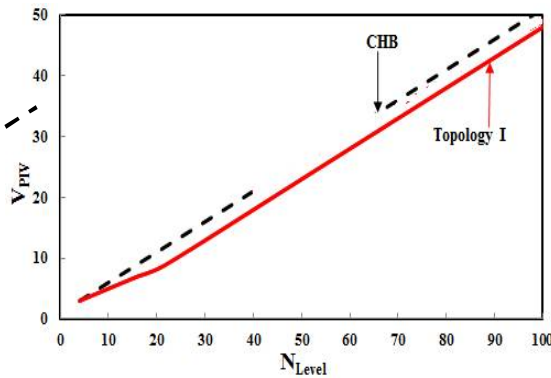


Fig.4a Comparison of Number of Level against Peak inverse voltage

IV. SIMULATION RESULT

In this paper, symmetric multilevel inverters were presented. It was shown that the proposed symmetric topology needs fewer numbers of power electronic components in comparison with othersimilar topologies. Moreover, the experimental results for a 15-level hybrid topology were shown. It was shown that the simulation and experimental results have good agreement to each other. To verify authority of proposed multilevel inverter is simulated using computer based simulation (MATLAB/SIMULINK). Each dc source of voltages $V_1=V_2=V_3=V_4=V_5=V_6=66V$. The sum of all magnitudes values 330V which produce rms voltage of 230V. Load parameters: $R=20\Omega$, $L=100e^{-3}$. The value of output voltage frequency is 50Hz. Modulation strategies are used in cascaded multilevel inverter to reduce the harmonic content. The pulse width modulation method is used in the proposed multilevel inverter because fixed dc input voltage, is supplied to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter power semiconductor devices. Fig.6 shows that the simulation circuit diagram.

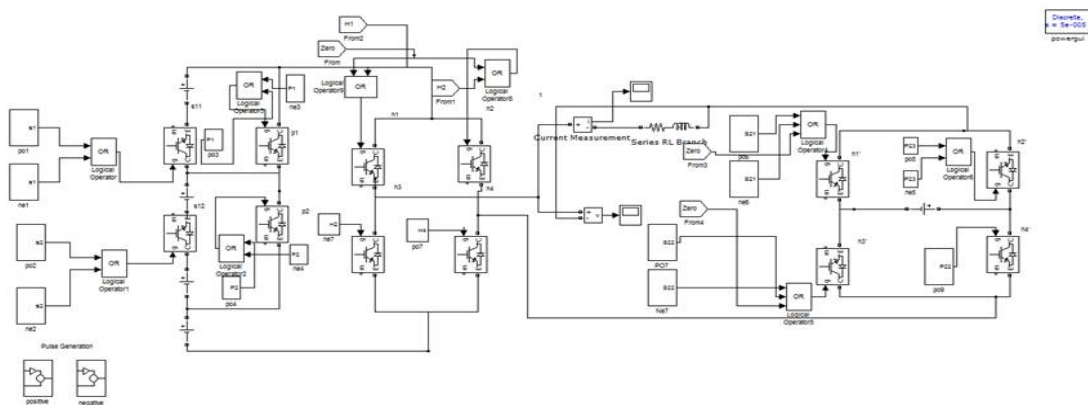


Fig.6 Simulation circuit

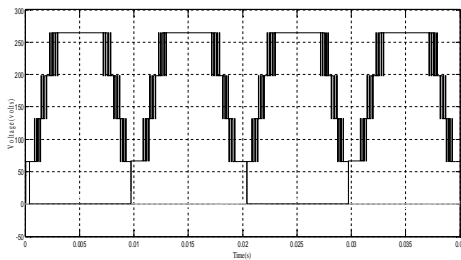


Fig.8 Output pulse for DE- MUX

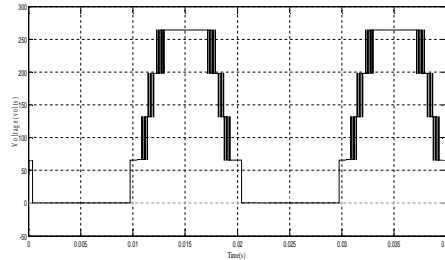


Fig. 9 V_{0max} of SDMLI

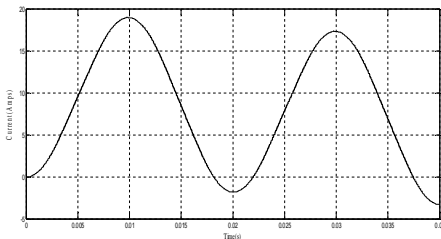


Fig. 10 Output pulse current given to

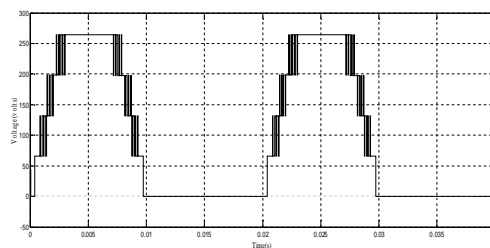
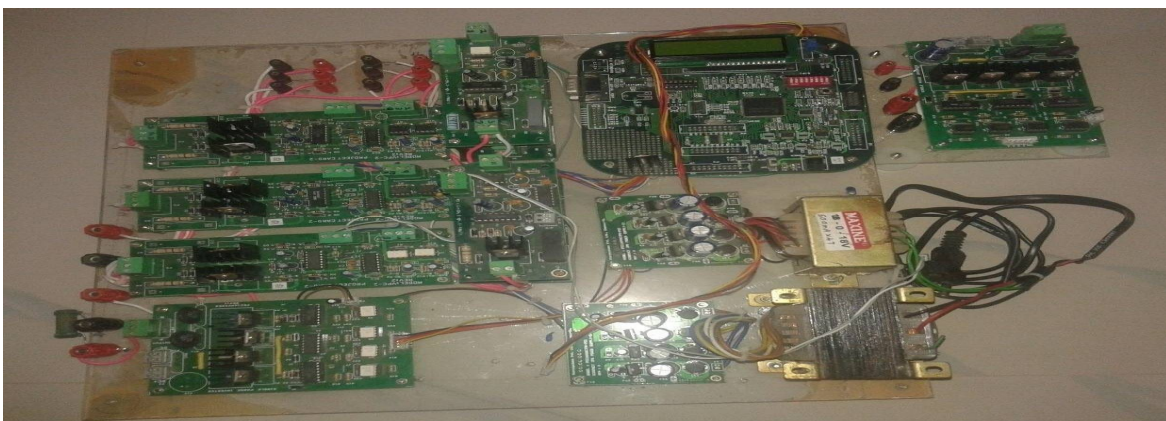


Fig. 11 V_{0max} of Packed H Bridge Switches

V. PROTOTYPE MODEL

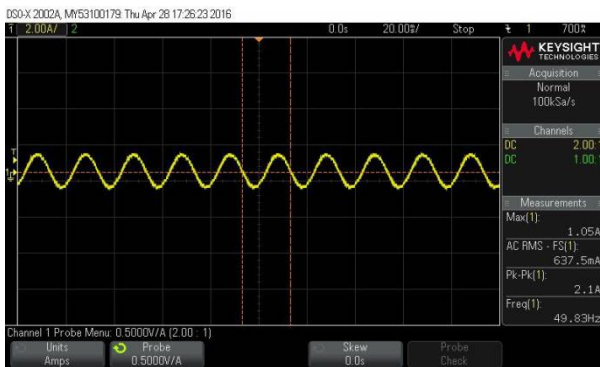
In this section, the simulation and experimental results for three topologies square measure provided. Firstly, the simulation results for 9-level symmetric topology square measure bestowed.. Finally, the simulation results for 11-level hybrid topology based on second method square measure bestowed. For all of the studies, Tests have been made on the R-L load with the magnitude of 30 mH and two hundred Ω . The value of output voltage frequency is 50 rate. For simulation, the MATLAB/Simulink software is used. It is noticeable that the fundamental frequency-switching technique is applied to the new topologies to trigger the power switches for controlling the voltage levels generated on the output.



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VI.CONCLUSION

In this paper, the novel symmetric multilevel inverter is proposed. This multilevel inverter can be implemented in industrial where the minimum switches are required. A generalised multilevel inverter using a multilevel inverter with maximum blocking voltage was simulated and output waveform were observed using MATLAB software. This proposed system use a five dc sources and twelve switches. A fundamental switching frequency control was used to shows the proposed eleven level output waveform. There by THD and switches were reduced.as the level can increase pure sine wave can be achieved. The voltage output and current is verified to confirm the performance of proposed multilevel inverter. The nearest level modulation technique is implemented. Future work on this proposed topology considers: (i) High voltage applications by cascading the proposed topology. (ii) In practical applications such as, Induction motor drives and FACTS controllers.

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